Fabrication and Characterization of Novel Photodefined Polymer-Enhanced Through-Silicon Vias for Silicon Interposers

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Abstract

To attain high bandwidth communication between chips at lower power consumption, silicon interposers with dense metallization and through-silicon vias (TSVs) have been widely explored. However, TSV electrical losses increase as TSV height increases and are generally high in low-resistivity silicon. To alleviate this issue, we demonstrate a silicon interposer technology featuring photodefined polymer embedded vias. High-frequency measurements are performed for the fabricated polymer-embedded vias, yielding approximately 1 dB insertion loss at 50 GHz.

I. Introduction

The migration to multicore, and eventually many-core, microprocessors has created an incredible demand for low-energy and massive off-chip bandwidth communication. This interconnection need has motivated significant disruptive research in the area of novel system-level interconnects [1]. To attain high bandwidth communication between chips at reduced energy, 3-dimensional (3D) chip integration has been widely explored [1-3]. Moreover, silicon interposers with through-silicon vias (TSVs) and high density metallization provide high bandwidth-density communication between assembled single and 3D ICs. N. Kim et al. [4] have demonstrated a silicon interposer with 10 µm diameter and 100 µm tall TSVs along with their high-frequency characterization. Using a 1 cm long channel with 2 μm^2 wiring cross-section and 8 µm channel pitch, Dickson et al. [5] have demonstrated 10 Gb/s per channel over a silicon interposer at 7.6 dB channel loss (at Nyquist) and energy efficiency of 5.3 pJ/bit. However, there are challenges for TSVs in silicon interposers. First, to obtain increased functionality (integration), a larger interposer is preferred, but the larger interposer requires thicker silicon for mechanical stability [6]; the thicker silicon necessitates longer TSVs, which will exhibit greater electrical losses [7]. Moreover, TSV electrical losses increase as silicon resistivity reduces [8]. Reduction in TSV losses has been shown in the literature using 1) high resistivity silicon [8], 2) alternative interposer technologies such as glass or dielectric interposers [8-10], 3) TSVs with thick dielectric liner [11, 12], and 4) coaxial TSVs [8]. However, high resistivity silicon is expensive. Moreover, via fabrication in glass is still in development and glass suffers from poor thermal conductivity.

To reduce TSV electrical losses and consequently implement longer TSVs for larger and thicker interposers using low resistivity (economical) silicon, this paper demonstrates novel photodefined polymer-embedded vias along with their dimensional scaling and high-frequency characterization. As shown in Figure 1, polymer-embedded vias consist of copper vias embedded within photodefined polymer wells in low resistivity silicon.

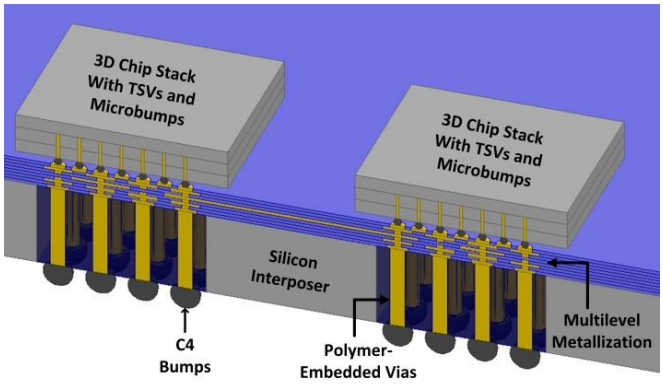
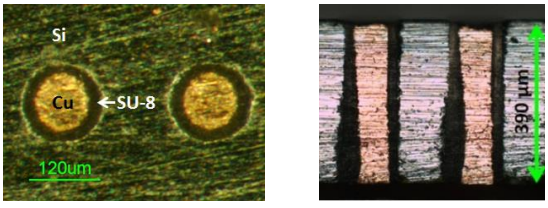


Figure 1: Cross section of a silicon interposer with polymer-embedded vias and 3D ICs atop the interposer

Compared to conventional TSVs, since a dielectric (polymer) separates the copper vias, instead of silicon and thin silicon dioxide liner, a reduction in TSV high-frequency losses can be expected for the polymer-embedded vias [8-10]. T. G. Lim et al. [10] simulated electrical loss of copper coated silicon pillars within a polymer cavity in silicon and compared to conventional TSVs to demonstrate improved performance. Moreover, since the polymer-embedded vias are fabricated using photodefinition, the need for advanced or expensive silicon etching technologies reduces. However, there is a minimal body of work on the fabrication of TSVs using photodefinition and polymer enhancement. S. W. Ho et al. [13] demonstrated coaxial TSVs fabricated using photodefinition of polymer filled vias supported by a temporary release film. Additionally, to reduce TSV losses and stresses, previously we demonstrated the fabrication of photodefined polymer-clad TSVs (80 µm diameter and 390 µm tall copper vias with a 20 µm thick polymer liner between the copper and silicon (Figure 2)) [11].



(a) Top View (b) Cross-Section View

Figure 2: (a) Top view and (b) Cross section view of 390 µm tall polymer-clad TSVs with 80 µm diameter copper vias surrounded by a 20 µm thick cladding on a 250 µm pitch [11]

In this work, we explore the use of polymer-embedded vias to improve electrical performance. To better illustrate the formation of photodefined polymer-embedded vias compared to other competing TSV technologies, Figure 3 schematically illustrates conventional TSVs, polymer-clad TSVs and polymer-embedded vias with the same diameter copper vias.

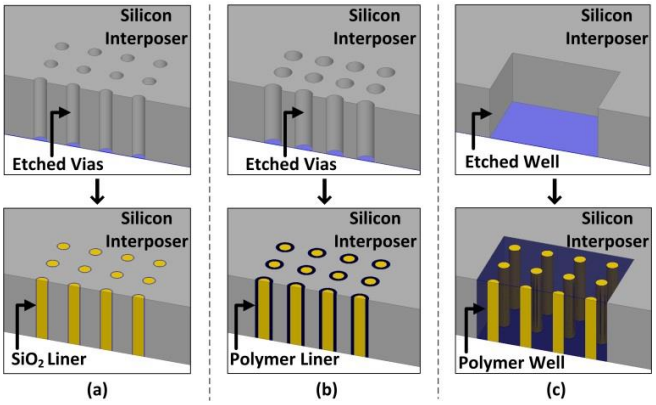


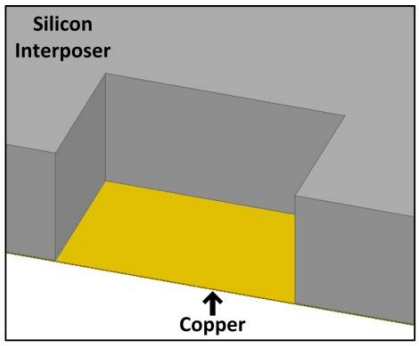
Figure 3: Schematic comparing three competing TSV technologies: (a) conventional TSVs with silicon dioxide liner, (b) polymer-clad TSVs and (c) polymer-embedded vias

II. TSV Fabrication

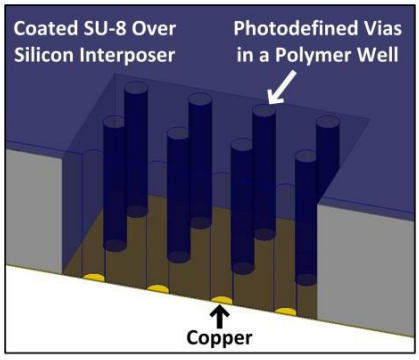
The fabrication process for the polymer-embedded vias is shown in Figure 4. First, silicon dioxide, titanium and copper are deposited on one side of a silicon wafer. Next, wells are etched in the silicon using the Bosch process [14] followed by etching of silicon dioxide and titanium at the bottom of the wells using buffered oxide etch (BOE). Next, SU-8 coating and soft bake are performed followed by ultraviolet (UV) exposure. Optimum exposure dose was obtained through design of experiments [15]. Next, post exposure bake is performed followed by development with ultrasonic agitation and isopropanol clean, yielding vias in the SU-8-filled wells. Next, bottom-up copper electroplating is performed using Microfab DVF 200 MU solution from Enthone followed by chemical mechanical polishing (CMP) using iCue 5001 slurry from Cabot Microelectronics Corporation to remove overburden copper. Using this fabrication process, polymer-embedded vias were fabricated with the dimensions shown in Table 1.

As shown in Figure 5(a) and Figure 5(b), 270 µm tall and 100 µm diameter polymer-embedded vias on a 250 µm pitch were formed in 1 mm x 1 mm polymer-filled wells. To demonstrate via diameter scalability, 65 µm diameter copper vias were also formed, as shown in Figure 5(c). Fabrication of the scaled polymer-embedded vias was performed using the same fabrication process implemented for the 100 µm diameter TSVs.

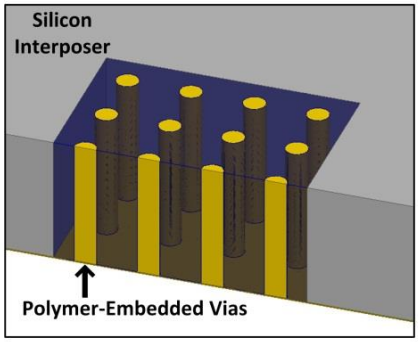
To confirm the high yield of the fabricated polymer-embedded vias, 4-point resistance measurements were performed, as shown in Figure 6. The fabricated TSVs were dipped in a 5% sulfuric acid solution before resistance measurements. The average measured resistance for 20 polymer-embedded vias with 100 µm diameter was 2.54 mΩ, and the average measured resistance for 20 polymer-embedded vias with 65 µm diameter was 2.77 mΩ.



1. SiO_2, Ti and Cu Deposition Followed By Si Etching Using Bosch Process and SiO_2 and Ti Wet Etching



2. SU-8 Coating Followed By Photodefinition of Vias

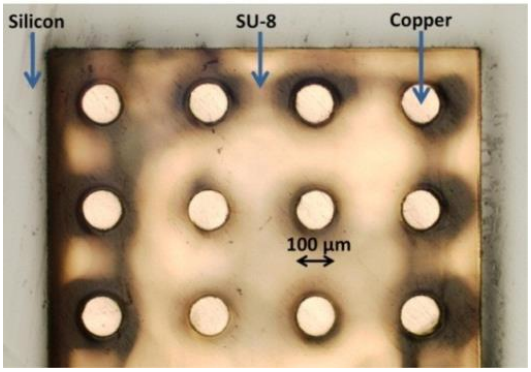


3. Cu Electroplating and CMP

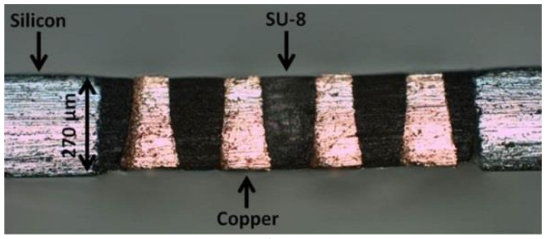
Figure 4: Fabrication process for polymer-embedded vias

Table 1: Fabricated polymer-embedded vias

Parameter	TSV Set #1	TSV Set #2
Diameter	100 µm	65 µm
Height	270 µm	270 µm
Pitch	250 µm	250 µm
Aspect Ratio	2.70	4.15
Polymer Well	1 mm x 1 mm	1 mm x 1 mm



(a)



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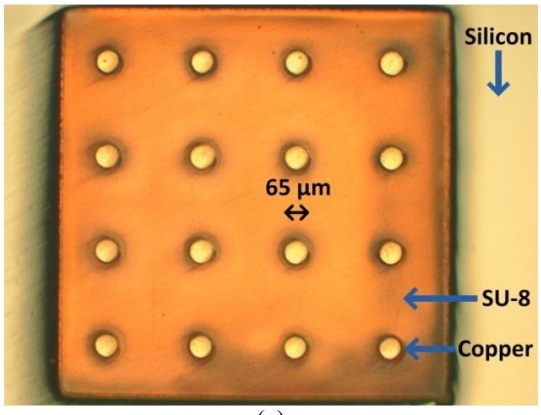
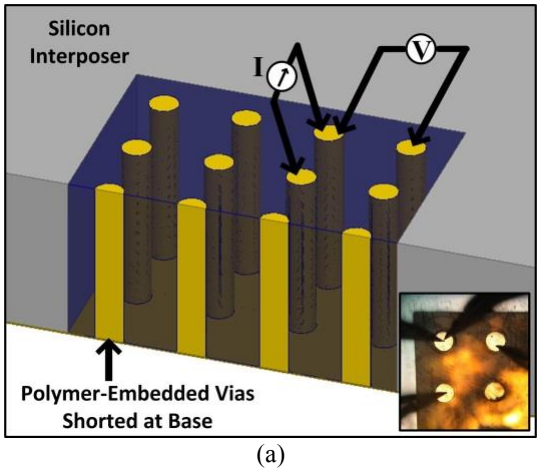
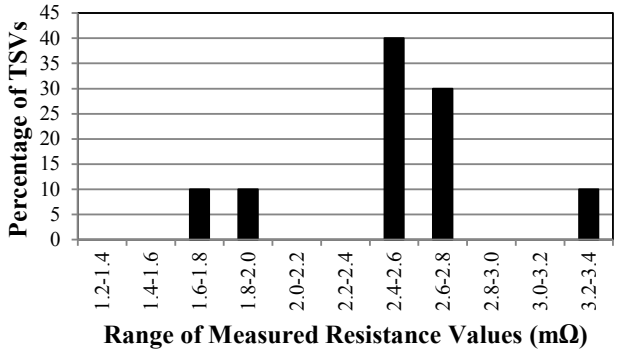


(c)

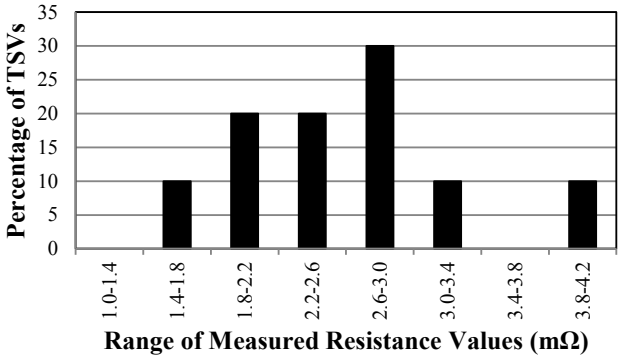
Figure 5: Fabricated 270 µm tall polymer-embedded vias on a 250 µm pitch: a) top view of 100 µm diameter TSVs, b) cross section view of 100 µm diameter TSVs, and c) Top view of 65 µm diameter TSVs



(a)



(b)



(c)

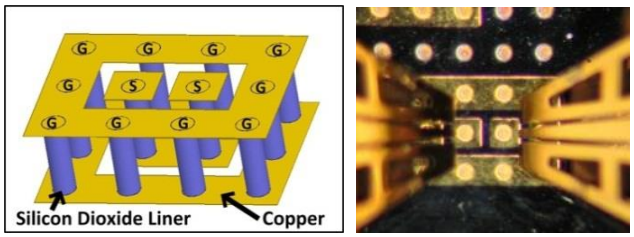
Figure 6: Four-point resistance measurement of 20 fabricated polymer-embedded vias: a) schematic with an inset image of the TSVs being measured, b) distribution of the measured resistance values of 100 µm diameter vias, and c) distribution of the measured resistance values of 65 µm diameter vias

III. TSV High-Frequency Measurements

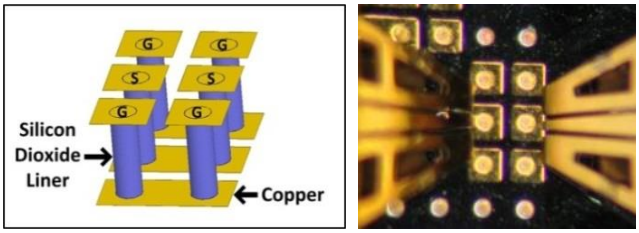
Before fabricating the test structures for high-frequency characterization of the polymer-embedded vias, two measurement structures, with signal traveling from a via-trace-via path in each structure, were first investigated for wafer level high-frequency characterization of conventional TSVs with silicon dioxide liner (Figure 7). Structure A is similar to [4] where all the ground vias are shorted from top as well as base, whereas in structure B, the ground vias and traces run parallel to the signal vias and traces. The two structures were first fabricated using 88 µm diameter and 290 µm tall conventional TSVs on a 250 µm and with a 1 µm thick silicon dioxide liner, as shown in Figure 7. The metal traces connecting TSVs are 190 µm wide and 1 µm thick with a 2.5 µm thick silicon dioxide layer insulating the silicon from the metal traces.

First, full wave electromagnetic simulations were performed in High Frequency Structure Simulator (HFSS) with 11.68 and 3.9 as the relative dielectric constants of silicon and silicon dioxide, respectively [16]. Next, for the high-frequency measurements up to 50 GHz, a dedicated RF probe station setup was used with Agilent N5245A PNA-X network analyzer and Cascade |Z| Probes. Prior to the measurements of the TSVs, LRRM calibration protocol was

implemented to de-embed the measurements of the device under test. Once the setup was calibrated, high-frequency measurements were performed for the conventional TSVs, as shown in Figure 8. Similar loss profiles were observed in both the measured structures.



(a) Structure A: Schematic (Left) and Measurement (Right)



(b) Structure B: Schematic (Left) and Measurement (Right)

Figure 7: Investigated structures for high-frequency measurements of the fabricated conventional TSVs with silicon dioxide liner

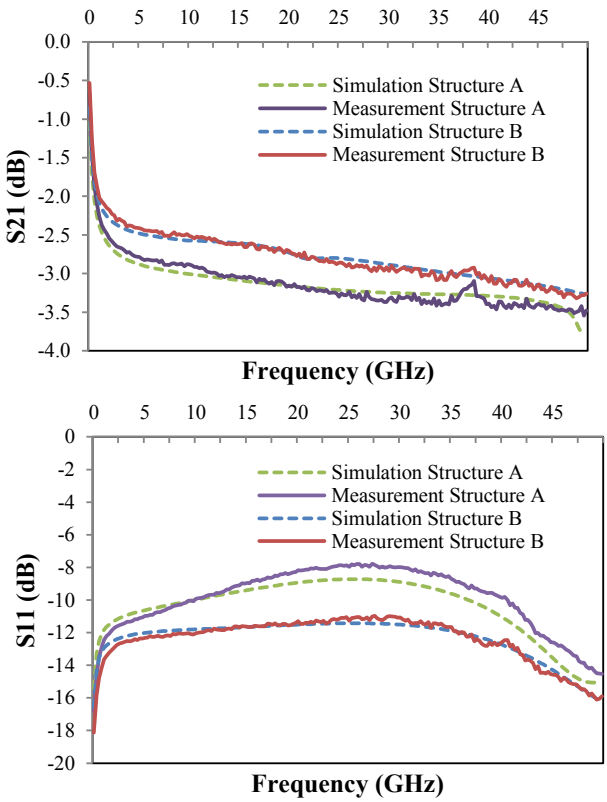


Figure 8: Simulated and measured losses for the fabricated conventional TSV structures (as shown in Figure 7) with silicon dioxide liner

As shown in Figure 9, Structure B was implemented for high-frequency measurements of the fabricated 65 µm diameter polymer-embedded vias. An X-ray image of the fabricated polymer-embedded vias with metallization for the high-frequency measurements is also shown. Figure 10 demonstrates high-frequency simulations and measurements of the fabricated polymer-embedded vias. Full wave electromagnetic simulations were performed in HFSS from 100 MHz to 50 GHz with 3.25 and 0.035 as the relative dielectric constant and the loss tangent of SU-8, respectively [13]. Prior to TSV measurements, calibration was performed as explained earlier. The measured insertion loss was approximately 1 dB at 50 GHz.

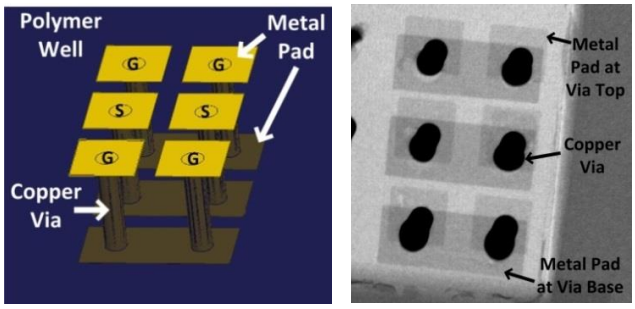


Figure 9: GSG TSV structure schematic (left) and x-ray image (right) of 65 µm diameter polymer-embedded vias with metallization

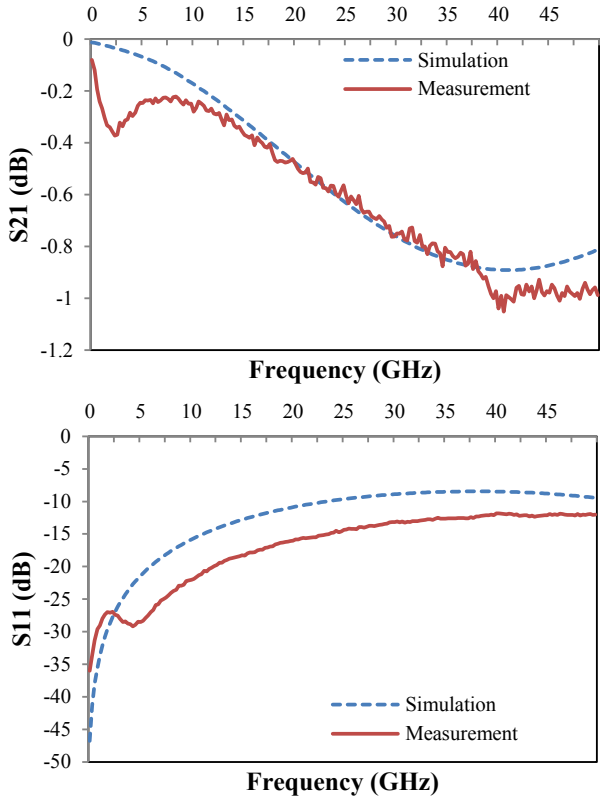


Figure 10: High-frequency simulation and measurement results for the fabricated 65 µm diameter polymer-embedded vias with via-trace-via structure

IV. Conclusion

The paper demonstrates fabrication and characterization of novel photodefined polymer-embedded vias for silicon interposers. Since a dielectric separates the copper vias, improved electrical performance can be obtained compared to conventional TSVs. Additionally, since the fabrication is assisted by photodefinition, the requirement of expensive silicon etching technologies is reduced. Resistance measurements were performed to confirm the high fabrication yield. Finally, high-frequency simulations and measurements were performed for the fabricated polymer-embedded vias.

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References

[1] M. S. Bakir and J. D. Meindl, Integrated Interconnect Technologies for 3D Nanoelectronic Systems, Artech House, 2009.

[2] J. U. Knickerbocker, P. S. Andry, B. Dang, R. Horton, C. Patel, R. Polastre, K. Sakuma, E. Sprogis, C. Tsang, B. Webb, and S. Wright, "3D silicon integration," in *Proc. 58th IEEE Electronic Components and Technology Conference (ECTC)*, Lake Buena Vista, FL, USA, 2008, pp. 538–543.

[3] J. U. Knickerbocker, P. S. Andry, E. Colgan, B. Dang, T. Dickson, X. Gu, C. Haymes, C. Jahnes, Y. Liu, J. Maria, R. J. Polastre, C. K. Tsang, L. Turlapati, B. C. Webb, L. Wiggins and S. L. Wright, "2.5D and 3D technology challenges and test vehicle demonstrations," in *Proc. 62nd IEEE Electronic Components and Technology Conference (ECTC),* 2012, pp. 1068 - 1076.

[4] N. Kim, D. Wu, D. Kim, A. Rahman, and P. Wu, "Interposer design optimization for high frequency signal transmission in passive and active interposer using through silicon via (TSV)," in *Proc. 61st IEEE Electronic Components and Technology Conference (ECTC)*, Lake Buena Vista, FL, USA, 2011, pp. 1160–1167.

[5] T. Dickson, Y. Liu, S. Rylov, B. Dang, C. Tsang, P. Andry, J. Bulzacchelli, H. Ainspan, X. Gu, L. Turlapati, M. Beakes, B. Parker, J. Knickerbocker, and D. Friedman, "An 8x10-gb/s source-synchronous I/O system based on high-density silicon carrier interconnects," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 4, pp. 884–896, Apr. 2012.

[6] M. Sunohara, H. Sakaguchi, A. Takano, R. Arai, K. Murayama, and M. Higashi, "Studies on electrical performance and thermal stress of a silicon interposer with TSVs," in *Proc. 60th IEEE Electronic Components and Technology Conference (ECTC)*, 2010, pp. 1088–1093.

[7] J. S. Pak, C. Ryu, and J. Kim, "Electrical characterization of through silicon via (TSV) depending on structural and material parameters based on 3D full wave simulation," in *Proc. International Conference on Electronic Materials and Packaging (EMAP)*, Daejeon, South Korea, 2007, pp. 1–6.

[8] I. Ndip, B. Curran, K. Lobbicke, S. Guttowski, H. Reichl, K.-D. Lang, and H. Henke, "High-frequency modeling of TSVs for 3-d chip integration and silicon interposers considering skin-effect, dielectric quasi-TEM and slow-wave modes," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 10, pp. 1627–1641, Oct. 2011.

[9] T. Bandyopadhyay, R. Chatterjee, D. Chung, M. Swaminathan, and R. Tummala, "Electrical modeling of through silicon and package vias," in *Proc. IEEE International Conference on 3D System Integration (3DIC),* San Francisco, CA, USA, 2009, pp. 1-8.

[10] T. G. Lim, Y. M. Khoo, C. S. Selvanayagam, D. S. W. Ho, R. Li, X. Zhang, G. Shan, and X. Y. Zhong, "Through silicon via interposer for millimetre wave applications," in *Proc. 61st IEEE Electronic Components and Technology Conference (ECTC)*, Lake Buena Vista, FL, USA, 2011, pp. 577-582.

[11] M. Parekh, P. Thadesar, and M. Bakir, "Electrical, optical and fluidic through-silicon vias for silicon interposer applications," in *Proc. 61st IEEE Electronic Components and Technology Conference (ECTC)*, Lake Buena Vista, FL, USA, 2011, pp. 1992–1998.

[12] Y. –J. Chang, T. –Y. Zheng, H. –H. Chuang, C. –D. Wang, P. –S. Chen, T. -Y. Kuo, C. –J. Zhan S. –H. Wu, W. -C. Lo, Y. –C. Lu, Y. –P. Chiou, and T. –L. Wu, "Low slow-wave effect and crosstalk for low-cost ABF-coated TSVs in 3-D IC interposer," in *Proc. 62nd IEEE Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, 2012, pp. 1934–1938.

[13] S. W. Ho, S. W. Yoon, Q. Zhou, K. Pasad, V. Kripesh, and J. H. Lau, "High RF performance TSV silicon carrier for high frequency application," in *Proc. 58th IEEE Electronic Components and Technology Conference (ECTC)*, 2008, pp. 1946–1952.

[14] B. Wu, A. Kumar, and S. Pamarthy, "High aspect ratio silicon etch: A review," *Journal of Applied Physics*, vol. 108, no. 5, pp. 051 101–051 101–20, Sep. 2010.

[15] P. Thadesar and M. Bakir, "Novel photodefined polymer-embedded vias for silicon interposers," *Journal of Micromechanics and Microengineering*, vol. 23, no. 3, pp. 035003-1–035003-6, 2013.

[16] J. Robertson, "High dielectric constant oxides," *The European Physical Journal Applied Physics*, vol. 28, no. 3, pp. 265–291, Dec. 2004.